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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,685	04/01/2004	Jeffrey Orion Pritchard	ALTRP117/A1404	1625

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/816,685	PRITCHARD ET AL.
	Examiner	Art Unit
	Helen Rossoshek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 20-30* is/are rejected.

7)☒ Claim(s) *17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/9/05,2/1/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/816,685 filed 04/01/2004.

2. Claims 1-30 are pending in the Application.

Drawings

3. The drawings are objected to because Element **709** is missed on the Figure 7, while it is mentioned in the description of the Figure 7 in the Specification on the page 20. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 6, 8, 26 and 28 are objected to because of the following informalities: there is insufficient antecedent basis for this limitation in the claims. Are "pointer write access" (claim 6) and "a pointer read access" (claim 8) the same as "pointer read and write access" (claim 4)?

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-16 and 20-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Frankel et al. (US Patent Application Publication 20030093254).

With respect to claims 1 and 30 Frankel et al. teaches a method for implementing a programmable device within implementing programmable logic devices (PLDs) such ad field programmable gate arrays (FPGAs) (paragraph [0038]), a system for implementing a programmable device within a simulation system (paragraph [0008]), the method comprising: receiving a High-level language program, the high-level language program configured to run on a conventional central processing unit within representation of the model of the components of the integrated circuit design in the

hardware description language (HDL) (paragraph [0004]), wherein the model may be simulated, and simulation system (the model of the components presented in HDL) is running on the computer system (conventional CPU) (paragraphs [0006], [0030]), and wherein the model (26, 28, 30) may be coded in any desired programming language (paragraph 0056]); identifying a portion of the high-level language program for hardware acceleration within the emulator 36 shown on the Fig. 2 including hardware accelerator, wherein emulator 36 is capable of receiving a portion of HDL description (paragraph [0058); generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device within the emulator 36 shown on the Fig. 2 including hardware accelerator implemented on the FPGAs, wherein the portion of the HDL is mapped into the FPGAs (paragraph [0058]); and coupling the hardware acceleration logic to memory within the simulation process running on the general computer system using their memory (paragraph [0030]).

With respect to claim 20 Frankel et al. teaches a system for implementing a programmable device within a simulation system (paragraph [0008]), the system comprising: an interface operable to receive a high-level language program, the high-level language program configured to run on a conventional central processing unit within interface API 20 shown on the Fig. 2, node 12O, wherein hardware device 40 is implemented on the FPGA and the portion of HDL is mapped into FPGA (paragraph 0039]); a processor operable to identify a portion of the high-level language program for hardware acceleration and generate hardware acceleration logic for performing the portion of the high-level language program on the programmable device within the

emulator 36 shown on the Fig. 2 including hardware accelerator, wherein emulator 36 is capable of receiving a portion of HDL description (paragraph [0058) and is a part of the simulation process and simulation system (the model of the components presented in HDL) is running on the computer system (conventional CPU) (paragraphs [0006], [0030])).

With respect to claims 2-19 Frankel et al. teaches:

Claims 2 and 22: wherein generating hardware accelerator logic includes generating HDL within software included in emulator 36 shown on the Fig, 2 having hardware accelerator for receiving portion of the HDL for further mapping into the programmable device (paragraph [0058]);

Claims 3, 23: wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the programmable device within the device hardware 40, which may be the hardware implementing the portion of the system under test (model or components) (paragraph [0059]);

Claims 4, 24: wherein generating hardware acceleration comprises identifying pointer read and write access in the portion of the high-level language program using the simulating mechanism including software and hardware components for performing a simulation of the **portion** to the system under the test with an ability of the software to read and write in the file (e.g. source code) (paragraph [0015]);

Claims 5, 25: wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the

programmable device within mapping the description of the model into programmable device by hardware assistance to accelerate the simulation (paragraph [0058]);

Claims 6, 26: providing the hardware acceleration with a write port for a pointer write access identified in the portion of the high-level language program within an ability of the emulator 36 using the simulating mechanism including software and hardware components for performing a simulation of the **portion** to the system under the test with an ability of the software to read and write in the file (e.g. source code) (paragraph [0015]);

Claims 7, 27: wherein the write port includes a write address line having an address corresponding to the address of the pointer using the simulating mechanism including software and hardware components for performing a simulation of the **portion** to the system under the test with an ability of the software to read and write in the file (e.g. source code) (paragraphs [0015], [0039]));

Claims 8, 28: providing the hardware accelerator with a read port for a pointer read access identified in the portion of the high-level language program within an ability of the emulator 36 using the simulating mechanism including software and hardware components for performing a simulation of the **portion** to the system under the test with an ability of the software to read and write in the file (e.g. source code) (paragraph [0015]);

Claims 9, 29: therein the read port includes a read address line having an address corresponding to the address of the pointer within an ability of the emulator 36 using the simulating mechanism including software and hardware components for

performing a simulation of the **portion** to the system under the test with an ability of the software to read and write in the file (e.g. source code) (paragraphs [0015], [0064]);

Claim 10: wherein the hardware accelerator component is coupled to a simultaneous primary component fabric within the device hardware 40, which may be the hardware implementing the portion of the system under test (model or components) (paragraphs [0059], [0064]);

Claim 11: wherein the central processing unit is a general purpose processor within the model, which may be simulated, and simulation system (the model of the components presented in HDL) is running on the computer system (conventional CPU) (paragraphs [0006], [0030]);

Claim 12: wherein the central processing unit supports a general purpose instruction set within distributed simulation processors shown on the Fig. 1 (paragraph [0030]);

Claim 13: wherein the high-level language program is prepared in ANSI C (paragraph [0056]);

Claim 14: further comprising providing a processor core operable an a conventional central unit, the processor core configured for implementation on the programmable device (paragraph [0030]);

Claim 15: wherein the portion includes multiple disconnected sections of the high-level language program within the portion of HDL description before it is implemented on the PLD by mapping (paragraph [0058]);

Claim 16: wherein the portion is identified automatically during parsing of the hag-level language program within the distributed simulation system having multiple nodes shown on the Figs. 1 and 2 (paragraph [0008]), wherein any combination of the nodes may be included to form the distributed simulation system (paragraph [0046]);

Claim 21: wherein the processor is further configured to couple the hardware acceleration logic to memory within the simulation process running on the general computer system using their memory (paragraph [0030]).

Allowable Subject Matter

7. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach a portion of the high-level language program for hardware acceleration is identified automatically using profiling data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER